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Upgrades to Ensure Power Integrity for AI Servers Are Driving Development of Complementary Roles for Silicon Capacitors and MLCCs

Topology Research Institute

The need for power integrity in AI servers is extending from the board level directly into the package. This shift is driving a transition in capacitor technology, moving beyond a sole reliance on traditional multi-layer ceramic capacitors (MLCCs) toward a layered, complementary approach utilizing both silicon capacitors and MLCCs. While MLCCs remain the primary components for system-level decoupling, filtering, and voltage regulation across PCBs, VRMs, power shelves, and power modules, silicon capacitors offer distinct localized advantages. Their thin profile, low equivalent series inductance (ESL), excellent high-frequency characteristics, and stable capacitance under DC bias and temperature fluctuations make them ideal for near-die decoupling around GPUs, ASICs, HBMs, and within advanced packages. As AI accelerators increasingly adopt chiplets, HBM stacking, and high-power packaging, silicon capacitors are poised to become vital complementary components for package-level power integrity in AI and HPC applications.

Comparison Between MLCCs and Silicon Capacitors

Item	MLCC	Silicon Capacitor
Manufacturing Process	Ceramic dielectric and multi-layer stacking processes.	Silicon substrate, thin-film dielectric, and semiconductor processes.
Key Advantages	Low cost, mature supply chain, diverse capacitance and size options; ideal for mass deployment.	Ultra-thin profile, low ESL, excellent high-frequency characteristics; superior stability under temperature and DC bias variations.
Primary Deployment Locations	PCBs, VRMs, OAM boards, power shelves, power modules; used for board-level decoupling.	Alongside GPUs / CPUs / ASICs, bottom of silicon interposers, embedded in packaging substrates; used for near-die decoupling.
AI Server Role	Primary components for system-level and board-level power stability.	Complementary components for package-level and near-chip power integrity.
Growth Drivers	Increased power consumption per rack, growing overall MLCC usage, and demand for high-capacitance / high-voltage products.	Rise of chiplets, HBM, advanced packaging, and the strict need for low ESL and high-frequency decoupling.
Limitations	Restricted in high-frequency and near-die applications due to component height, placement distance, and parasitic inductance.	Higher costs, heavy reliance on customization, smaller supply scales, and longer product qualification (validation) cycles.
DC Bias and Temp Stability	Capacitance may drop significantly under high DC bias or elevated temperatures; actual effective capacitance requires derating evaluation.	Capacitance is highly resistant to DC bias and temperature fluctuations; ideal for stable decoupling in near-die, high-frequency, and high-temperature environments.

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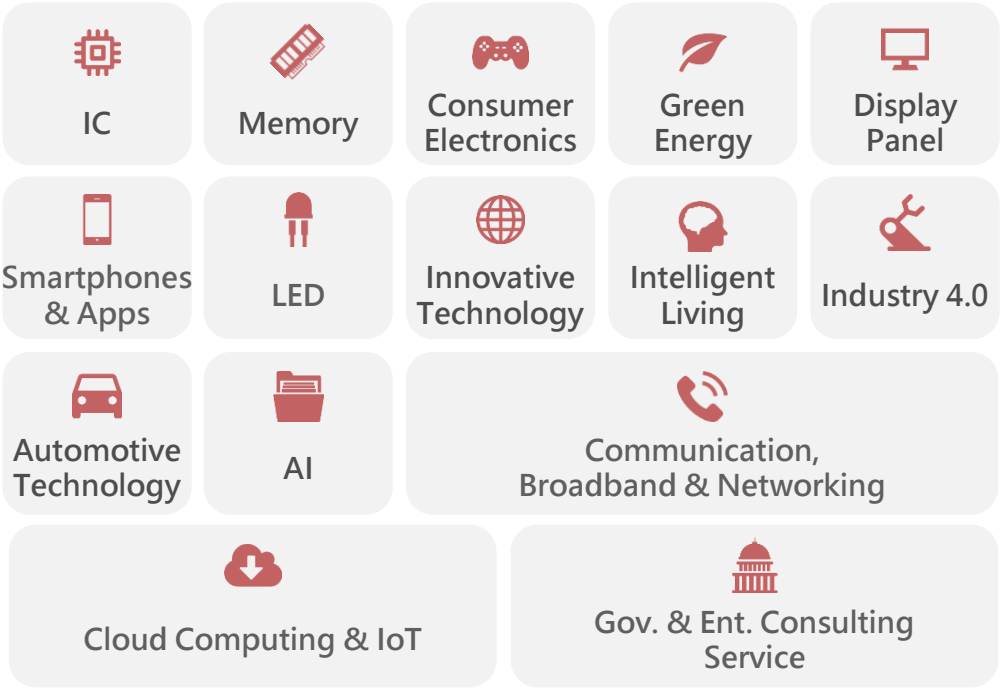

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